CLAIM AMENDMENTS

Please amend claim 66, without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment.

1-62. (Cancelled)

63. (Previously presented) A semiconductor disk device, comprising:

a non-volatile, electronically programmable and erasable flash memory, the flash memory being erasable by blocks,

interface means for exchanging data and addresses with an external system,

flash control buffer means for performing data exchange between the flash memory and the interface means, and

access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address.

64. (Previously presented) The semiconductor disk device according to claim 63, wherein

said flash memory includes a plurality of blocks , each block comprising an area for storing an address of another block and an area for storing data, and

said access means converts the sector address received from the external system into a substitute address and searches the block with such substitute address in order to read therefrom the number of another block.

65. (Previously presented) The semiconductor disk device according to either of claims 63 or 64, wherein the substitute address includes a logical block address.

66. (Currently amended) A semiconductor disk device, comprising:

a non-volatile, electronically programmable and erasable flash memory divided into a plurality of blocks containing memory cells that are erasable together, individual blocks including an area to store a block address and an area to store data,

an interface connected to exchange data and addresses with an external system,

a data buffer connected to the interface to exchange data between the flash memory and the interface,

addressing circuits responsive to a sector address received through the external system interface to (a) address a corresponding block, (b) read the block address stored in the block address area of said corresponding block, and (c) if the read block address is a match, addressing another block having the address read from said corresponding block.

67. (Previously presented) The semiconductor disk device of claim 66, wherein the flash memory includes an array of EEPROM cells that are individually programmable into exactly two states in order to store one bit of data per cell.

68. (Previously presented) The semiconductor disk device of claim 66, wherein the flash memory includes an array of EEPROM cells that are individually programmable into more than two states in order to store more than one bit of data per cell.

69. (Previously presented) In memory system that includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, a method of operating the memory system with a host computer, comprising:

configuring use of the memory cells within the individual sectors to provide at least distinct portions in which user data and a sector address are stored,

in response to receiving a memory address from the host computer, addressing a corresponding sector and reading the sector address from the sector address portion thereof,

if the read sector address is that of the addressed corresponding sector, sending data to the host computer that is read from the user data portion of the addressed corresponding sector, and

if the read sector address is that of a sector other than the addressed corresponding sector, addressing the other sector and sending data to the host computer that is read from the user data portion of the other sector.

70. (Previously presented) The method of claim 69, wherein the memory array is operated with the individual cells thereof being programmable into one of exactly two detectable states in order to store one bit of data per cell.

71. (Previously presented) The method of claim 69, wherein the memory array is operated with the individual cells thereof being programmable into one of more than two detectable states in order to store more than one bit of data per cell.

72. (Previously presented) The method of any one of claims 69-71, additionally comprising providing the memory array within a card that is removably connectable to the host computer system.

73. (Previously presented) The method of any one of claims 69-71, wherein the user data portion of the individual memory sectors has a capacity of 512 bytes of data.